

2010 Design and Verification Conference Attendee Questionnaire Results

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| | Percent |
|--|---------|
| Which is your primary design language? (Pick one) | |
| Verilog | 50% |
| VHDL | 8% |
| C/C++ | 13% |
| SystemC | 9% |
| SystemVerilog | 20% |
| Which primary verification language do you currently use? (pick one) | |
| C/C++ | 14% |
| e | 4% |
| OpenVera | 3% |
| Verilog | 25% |
| VHDL | 4% |
| SystemC | 9% |
| System Verilog | 41% |
| Which primary verification language do you plan to use for your next design? (Pick one) | |
| C/C++ | 13% |
| e | 3% |
| OpenVera | 2% |
| Verilog | 16% |
| VHDL | 3% |
| SystemC | 12% |
| SystemVerilog | 52% |
| Which primary property specification (assertion-based verification) language do you use or plan to use? | |
| Verilog | 28% |
| VHDL | 8% |
| PSL | 5% |
| SystemVerilog (SVA) | 59% |
| What design area(s) are you focused on? (Check all that apply) | |
| Systems Design | 11% |
| Standard ICs | 3% |
| ASICs | 16% |
| DSP Design | 4% |
| Microprocessor/Microcontroller Design | 6% |
| FPGAs & PLDs | 11% |
| Multi-Chip Modules | 3% |
| PCBs | 2% |
| Library Development | 2% |
| Analog/Mixed Signal | 4% |
| EDA Tools | 13% |
| Verification | 17% |
| SOCs | 9% |
| What on-chip buses do you intend to use in the next 12 months? | |
| AMBA 2.0 AHB/APB | 19% |
| AMBA 3 AXI | 16% |
| OCP 2.0 | 4% |
| OCP 2.1 | 6% |
| CoreConnect | 3% |
| Others/Proprietary | 21% |
| None | 30% |

| | Percent |
|---|---------|
| What standard interface do you expect to use in the next 12 months? | |
| PCI Express 1.1 | 5% |
| PCI Express 2.0 | 17% |
| USB 2.0/OTG | 13% |
| Serial ATA | 8% |
| 10G Ethernet | 8% |
| 10/100/1G Ethernet | 10% |
| Wireless USB | 6% |
| PCI/PCI-X | 7% |
| CE-ATA | 1% |
| None | 25% |
| What is the size in gates of your current/last design? (Pick one) | |
| Not Applicable | 37% |
| <1M | 10% |
| 1 - 3M | 10% |
| 3 - 5M | 5% |
| 5 - 10M | 11% |
| 10M - 50M | 15% |
| >50M | 12% |
| How many clock domains do your designs average? | |
| 1 | 4% |
| 2 | 8% |
| 2 - 5 | 26% |
| 5 - 10 | 18% |
| 10 - 20 | 7% |
| >20 | 6% |
| Not Applicable | 31% |
| What is your number one design constraint? | |
| Low power | 38% |
| Size/density | 13% |
| Performance/throughput | 49% |
| What are the two main reasons for your attendance at DVCon? | |
| Learn new techniques to improve your design process | 18% |
| Learn new methodologies to improve your verification process | 26% |
| Learn about new developments in design tools | 18% |
| Meet and network with other engineers in the industry | 24% |
| Learn about industry in general | 15% |
| Which category most closely describes your job description? (Pick one) | |
| Senior Management | 17% |
| Engineering Management | 18% |
| Design Engineer | 17% |
| System Architecture | 4% |
| Application Engineer | 4% |
| Marketing & Sales | 6% |
| Technical Marketing | 3% |
| Product Marketing | 3% |
| Sales | 3% |
| Research/Academic | 3% |
| CAD | 4% |
| Verification Engineer | 18% |