Press Release

DVCon 2012 Announces Best Paper Award and Record Attendance

Names Stan Krolikoski, Ph.D., General Chair for 2013

Louisville, CO – March 2, 2012 – The 20th annual Design and Verification Conference (DVCon), sponsored by Accellera Systems Initiative, wrapped up this week with continued growth in attendance and much enthusiasm from attendees. Overall attendance rose almost 10% to 834. Exhibits were sold out again this year with 35 exhibitors, 8 of them for the first time.

The Award for Best Paper, as voted by conference attendees, went to Erik Seligman, Dmitry Korchemny and Laurence Bisht, Intel Corp. for their paper, "SystemVerilog Assertion Linting: Closing Potentially Critical Verification Holes." Second prize went to Rich Edelman, Raghu Ardeishar and John Amouroux, Mentor Graphics Corp. for "Better Living Through Better Class-Based SystemVerilog Debug."

Two honorable mentions were awarded: "Yikes! Why is My SystemVerilog Testbench so Slow?" by Frank Kampf, IBM Corp. and Justin Sprague and Adam Sherer, Cadence Design Systems, Inc. and "Keeping Up with Chip - The Proposed SystemVerilog 2012 Standard Makes Verifying Ever-Increasing Design Complexity More Efficient" by Stuart Sutherland, Sutherland Hdl, Inc. and Tom Fitzpatrick, Mentor Graphics Corp.

"UVM continues to be a key driving factor and was a strong theme during DVCon again this year," according to Dr. Ambar Sarkar, DVCon Program Chair. "Coverage, re-use and verification IP continued as prominent themes, as well as ways to address verification challenges at the system level."

"There was definitely a buzz coming into DVCon this year," commented Karen Bartleson, DVCon General Chair. "I think attendees came in with high expectations and left feeling very satisfied. Our Technical Program Committee had outstanding submissions to choose from this year and they were able to expand the program to offer even more valuable content. There was also a lot of sharing of ideas and networking during the breaks, which has become a traditional and anticipated part of DVCon."

DVCon General Chair for 2013 will be Stan Krolikoski, Ph.D. He was previously the Tutorial and Panel Chair. Sarkar will continue as the Program Chair.

The poster sessions have become a mainstay of DVCon. This year attendees were crowded around the presentations, getting an up close opportunity for information gathering.

Other highlights of the week included the panel, "Build or buy: Which is the Best Practice for Hardware-Assisted Verification?" moderated by Brian Bailey. The Industry Leaders Panel, "The Resurgence of Chip Design," moderated by JL Gray, gave attendees a lot to ponder as the luminaries discussed how the need for increased collaboration between hardware and software teams is critical to the continued resurgence of chip design.

Accellera Systems Initiative Day was held on Monday to kick off the conference. There were also two co-located events, the EDAC Emerging Companies meeting and a presentation, "Do We Have What it Takes for Full-SoC Verification?" sponsored by Breker Verification Systems.

The Steering Committee values all feedback regarding the conference. Attendees have been given a survey and are asked to provide input on how to make DVCon 2013 even better.

About DVCon

DVCon is the premier conference for discussion of the functional design and verification of electronic systems. DVCon is sponsored by **Accellera Systems Initiative**, an industry consortium dedicated to the development and standardization of design and verification languages. For more information about Accellera, please visit www.accellera.org. For more information about DVCon, please visit www.dvcon.org. Follow @dvcon on Twitter or to comment, please use #dvcon.

For more information, please contact:

Kathy Embler
MP Associates, Inc.
303-530-4562
kathy@mpassociates.com

Barbara Benjamin
HighPointe Communications
503-209-2323
barbara@hipcom.com