Calypto Participating in Tutorial on Pre-simulation Verification for RTL Sign-off and Exhibiting at DVCon 2013

SAN JOSE, Calif., – February 21, 2013 – AT DVCon 2013, Calypto® Design Systems, Inc., the leader in electronic system level (ESL) hardware design and register transfer level (RTL) power optimization, will participate in a tutorial on pre-simulation verification for RTL sign-off and exhibit its best-in-class tools for power optimization, functional verification and ESL synthesis. Calypto empowers designers to create high quality, low power ASIC and FPGA hardware products. Calypto's three product families (PowerPro®, Catapult® and SLEC®) offer customers solutions ranging from RTL power reduction to C++/ SystemC high-level synthesis.

WHAT: Demonstrating and presenting on PowerPro, Catapult and SLEC in the Calypto booth. Participating in Tutorial Session 10: Pre-simulation Verification for RTL Sign-off [sponsored by Real Intent]. The presentation will cover power exploration, analysis and optimization using an abstract model with high-level synthesis (HLS), followed by the RTL static verification for: syntax and semantic checking (lint); constraints planning and management; reset analysis and optimization; automatic intent verification; CDC sign-off; DFT analysis and insertion; and X-analysis and optimism/pessimism correction. Each step represents a substantial hardening of the design and is best served by a top-of-the-line tool designed specifically for that step. Speakers include:

Chouki Aktouf - *DeFacTo Technologies*
Pranav Ashar - *Real Intent, Inc.*
Bryan Bowyer - *Calypto Design Systems, Inc.*

For additional details, see DVCon Tutorial.

WHERE: Doubletree hotel, San Jose, California.

Calypto will provide live demonstrations at booth #705.

Tutorial 10 will take place in the Santa Clara Room.

WHEN: The exhibition floor at DVCon 2013 is open from 3:30-6:30pm on February 26th and 27th .

Tutorial 10 runs from 1:30-5:00pm on Thursday, February 28th

About Calypto's Products

Catapult high level synthesis, Calypto's SLEC (sequential logic equivalence checking) and PowerPro platforms are used by seven out of the top ten semiconductor companies and over 100 leading consumer electronics companies worldwide. Calypto's products enable electronic system level design by engineers to dramatically improve design quality and reduce power consumption of their system-on-chip (SOC) devices.

About Calypto

Calypto® Design Systems, Inc. is the leader in ESL hardware design and RTL power optimization. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the ARM Connected Community, Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America.

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