Calypto's Catapult Integrates with Real Intent's Ascent Lint for Reliable RTL Implementation Flow

SAN JOSE and SUNNYVALE, Calif., – February 11, 2013 – Calypto® Design Systems, Inc., the leader in Electronic System Level (ESL) hardware design and Register Transfer Level (RTL) power optimization, and Real Intent, Inc., the leading provider of software products that accelerate early functional verification and advanced sign-off of electronic designs, today announced the integration of Calypto's Catapult high-level synthesis tool and Real Intent's Ascent™ Lint product. The resulting solution ensures Catapult-generated RTL code is lint clean and error free for a safe and reliable implementation flow from RTL to GDSII layout.

"A key requirement for our customers is to seamlessly fit within existing design flows," said Shawn McCloud, Vice President of Marketing at Calypto. "More customers are moving to C++ or SystemC as an input language for hardware design where verification can be performed more exhaustively and up to 10,000X faster than RTL. Catapult Synthesis delivers the link from these abstract models to RTL, and integrating it with Real Intent's RTL linter ensures an error-free design flow for today's complex SoCs."

"By delivering high performance, capacity and low-noise reporting, Ascent Lint is a state-of-the-art RTL linter and rule checker for full-chip SoC analysis," said Graham Bell, Sr. Director of Marketing, Real Intent. "Ascent Lint verifies RTL designs in minutes, which is nearly 50X faster than older lint tools. By integrating with Calypto's synthesis tool, we enable designers to quickly go from ESL to gates, secure in the knowledge that their RTL code meets all of the industry quality standards in their implementation flow."

About Calypto's Products

Catapult High Level Synthesis, Calypto's SLEC (Sequential Logic Equivalence Checking) and PowerPro platforms are used by seven out of the top ten semiconductor companies and over 100 leading consumer electronics companies worldwide. Calypto's products enable electronic system level design by engineers to dramatically improve design quality and reduce power consumption of their system-on-chip (SoC) devices.

About Real Intent's Products

Real Intent offers two product families – Ascent for early functional verification of RTL prior to synthesis; and Meridian for advanced sign-off verification of both CDC and timing constraints (SDC). Real Intent's products lead the market in performance, capacity, accuracy and completeness.

About Calypto

Calypto Design Systems, Inc. is the leader in ESL hardware design and RTL power optimization. Calypto, whose customers include Fortune 500 companies worldwide, is a member of the ARM Connected Community, Cadence Connections program, the IEEE-SA, Synopsys SystemVerilog Catalyst Program, the Mentor Graphics OpenDoor program, Si2 and is an active participant in the Power Forward Initiative. Calypto has offices in Europe, India, Japan and North America. More information can be found at www.calypto.com.

About Real Intent

Companies worldwide rely on Real Intent's EDA software to accelerate early functional verification and advanced sign-off of electronic designs. The company provides comprehensive CDC verification, advanced RTL analysis and sign-off solutions to eliminate complex failure modes of SoCs. Please visit www.realintent.com for more information.

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High-level synthesis
HLS
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