



## Media Advisory

### Atrenta to Present Assertion Synthesis Tutorial at DVCon 2013

**What:**

Yuan Lu, Chief Verification Architect at Atrenta and inventor of Assertion Synthesis, will present a tutorial at DVCon 2013 entitled: "Visibility into the Functional Verification Process using Assertion Synthesis"

**Who:**

Yuan Lu - Atrenta Inc.

John Henri Jr. - Cadence Design Systems, Inc.

Baosheng Wang - Advanced Micro Devices, Inc.

**When:**

Thursday, February 28, 2013

1:30PM - 5:00PM | DONNER BALLROOM

**Where:**

DVCon 2013, DoubleTree Hotel, San Jose, CA

**Why:**

This tutorial consists of an overview of Assertion Synthesis by its inventor, along with use models and in-depth discussions of methodologies for Assertion Synthesis deployment at different stages in the verification cycle. Cadence Design Systems will

participate, explaining how assertions, code and functional coverage at the sub-system and system level can be used to improve coverage closure and raise the level of design confidence prior to tape-out. AMD will also participate and share their experiences using assertions in areas such as performance modeling and emulation.

**Notes:**

For more details visit

[http://dvcon.org/2013\\_event\\_details?id=144-8-T](http://dvcon.org/2013_event_details?id=144-8-T)

**About Atrenta**

Atrenta's SpyGlass® Predictive Analysis software platform significantly improves design efficiency for the world's leading semiconductor and consumer electronics companies. Patented solutions provide early design insight into the demanding performance, power and area requirements of the complex system on chips (SoCs) fueling today's consumer electronics revolution. More than two hundred companies and thousands of design engineers worldwide rely on SpyGlass to reduce risk and cost before traditional EDA tools are deployed. SpyGlass functions like an interactive guidance system for design engineers and managers, finding the fastest and least expensive path to implementation for complex SoCs.

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