

For Immediate Release

Press Release

DVCon 2013 Announces Keynote, Final Program, Executive Panel Lineup
Accellera Systems Initiative Day will kick off conference

Louisville, CO – February 12, 2013 – The 2013 Design and Verification Conference (DVCon), sponsored by Accellera Systems Initiative, announced today the keynote and panelists for the Industry Leaders panel. DVCon also announced that the final program will be available online on February 14. DVCon 2013 will be held February 25 - 28 at the DoubleTree Hotel in San Jose, California.

Celebrating its 25th year, DVCon began as the VHDL Users Group in 1988 and has evolved to become the industry's premier conference for the discussion of functional design and verification of electronic systems. The keynote address for the 2013 conference, "Accelerating EDA Innovation through SoC Design Methodology Convergence," will be presented by Wally Rhines, chairman and CEO of Mentor Graphics, and will be held on Tuesday, February 26th at 3:30pm in the Oak/Fir Ballroom.

The Industry Leaders panel, "The Road to 1M Design Starts," will be moderated by JL Gray, vice president at Verilab and author of the "Cool Verification" blog. It will be held Wednesday, February 27th at 3:30pm in the Oak/Fir Ballroom. Panelists include: Yervant Zorian, fellow and chief architect, Synopsys; Ziv Binyamini, corporate vice president, Systems and Software Solutions, Cadence Design Systems; Sunil Shenoy, corporate vice president, general manager, Visual and Parallel Computing Group, Intel Corporation; John Costello, vice president, IC Design, Altera; and Serge Leef, vice president, New Ventures, Mentor Graphics.

On Monday, Accellera Systems Initiative Day will kick off the conference with in-depth tutorials on UVM, UPF, SystemC and SystemVerilog. The Technical Excellence Award will be presented during the special Town Hall luncheon on that day. Attendees will have an opportunity to discuss their most important questions about standards in an open format with Accellera representatives.

Conference attendees can also look forward to 12 technical sessions, 2 panels, 26 poster presentations and 29 exhibitors throughout the conference. For the first time, an award for the Best Poster Presentation will join the Best Paper Award this year.

To visit with the exhibitors, the DVCon Expo will be open on Tuesday and Wednesday from 3:30-6:30pm. Poster sessions will be held on Tuesday from 10:30-11:30am.

To view the complete four day program, including more information on the keynote address, all of the technical sessions and sponsored tutorials, please visit the conference website at www.dvcon.org.

DVCon is the premier conference for discussion of the functional design and verification of electronic systems. DVCon is sponsored by **Accellera Systems Initiative**, an independent, not-for profit organization dedicated to creating design and verification standards required by systems, semiconductor, intellectual property (IP) and electronic design automation (EDA) companies. For more information about Accellera, please visit

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For more information, please contact:

Kathy Embler
MP Associates, Inc.
303-530-4562
kathy@mpassociates.com

Barbara Benjamin
HighPointe Communications
503-209-2323
barbara@hipcom.com