Janick Bergeron Receives Accellera Systems Initiative Technical Excellence Award

Mr. Bergeron will be recognized for contributions to UVM at DVCon on February 25, 2013

San Jose, California, USA**,** DVCon—21 February 2013—Accellera Systems Initiative (Accellera) announced today that Janick Bergeron, a member of the Verification Intellectual Property (VIP) Technical Subcommittee (TSC), is the recipient of the second annual Accellera Technical Excellence Award. The award is being presented at the Design & Verification Conference (DVCon) on *Accellera Systems Initiative Day,* February 25, 2013 at the DoubleTree Hotel in San Jose, California. The award recognizes both the outstanding achievements Janick has made to the organization's Universal Verification Methodology (UVM™) standardization effort and the many technical advancements that he brought to the field of functional verification methodology.

"The UVM standard is improving interoperability among verification tools," remarked Shishpal Rawat, Accellera chair. "Very early in his career, Janick established an independent verification reuse methodology rooted in a base-class library that would eventually be built on SystemVerilog. He collaborated with his competitors under a standardization banner to bring together the best of all ideas to establish and create the Universal Verification Methodology. Today, Janick's register/memory package forms a substantial portion of the current UVM code base. Accellera is pleased to recognize his contributions to verification reuse methodology and to UVM through this award."

"As an expert in hardware verification languages and methodologies, Janick's technical contribution and involvement in defining and implementing UVM has been instrumental to the roll-out and successful deployment of UVM methodology worldwide," said Mr. Hillel Miller, co-chair of the VIP-TSC and SOC IP verification and SOC emulation manager, Digital Networking, Freescale Semiconductor. "Janick's special contributions to adapting the Register Package to the UVM Base Class Library have enabled semi-automatic register verification, vertical reuse and standard verification flows, making UVM easy to adopt by most verification teams."

"I'm honored by this prestigious and distinctive award which not only represents the technical merit of what the Accellera VIP-TSC has achieved, but also the impact UVM has had in the industry in a relatively short time frame," acknowledged Janick Bergeron. "While this award highlights an individual, it embodies the unique working relationship, contributions and aptitude of the entire committee and its chairs. I am fortunate to be collaborating with so many talented experts."

Janick Bergeron is a Synopsys Fellow responsible for the development and specification of functional verification methodology and management. Mr. Bergeron previously held several key engineering contributor positions at Qualis Design in Oregon and Nortel Networks in Ottawa, Ontario, Canada. He has consulted for dozens of leading technology companies in North America and Europe.

He is the author of the bestselling "Verification Methodology Manual for SystemVerilog" and of the "Writing Testbenches" book series. Both were the first industry references on modern functional verification techniques and methodologies. Mr. Bergeron has also authored over dozens of industry papers and over 10 training courses and tutorials in advanced verification and design methods. He is the founder and moderator of the Verification Guild, the most popular industry forum for discussing all aspects of functional verification.

About the Accellera Technical Committee

Accellera's Technical Committee oversees fourteen Working Groups that produce effective and efficient Electronic Design Automation (EDA) and Intellectual Property (IP) standards for today's advanced IC designs. Participants include member companies and industry contributors. Technical contributors typically have many years of practical experience with IC design and developing and using EDA tools. For a list of Accellera Working Groups, please click here.

About Accellera Systems Initiative

Accellera Systems Initiative (Accellera) is an independent, not-for profit organization dedicated to creating design and verification standards required by systems, semiconductor, intellectual property (IP) and electronic design automation (EDA) companies. The organization accelerates the development of standards that increase designer productivity and lower the cost of product development. As part of its ongoing partnership with the IEEE, standards developed by Accellera are contributed to the IEEE Standards Association for formal standardization and ongoing governance. For more information, visit www.accellera.org. For membership information, click here.

About DVCon

DVCon is the premier conference for discussion of the functional design and verification of electronic systems. DVCon is sponsored by Accellera Systems Initiative, an organization focused on the creation and adoption of EDA and IP standards. For more information, please visit www.accellera.org.
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Note to Editors
A photo is available on request.